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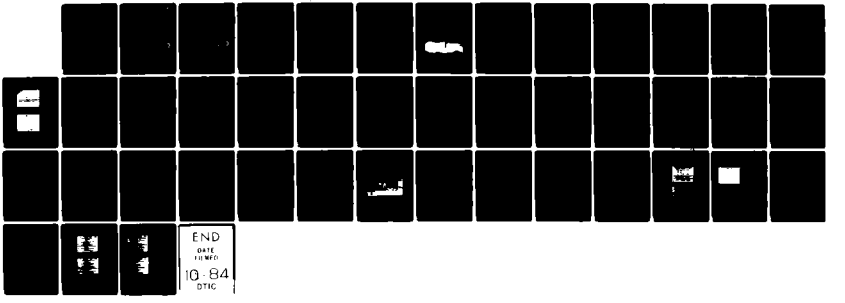

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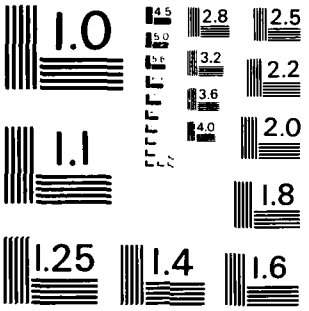

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ELECTRONIC BANDWIDTH COMPRESSION MODULE

FINAL REPORT

CONTRACT NO. N00173-80-C-0204

(G.O. 55769)

MARCH 1984

Presented To

DEPARTMENT OF THE NAVY

NAVAL RESEARCH LABORATORIES

WASHINGTON, D.C. 20375

By

WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER

SYSTEM DEVELOPMENT DIVISION

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P. O. BOX 1521

BALTIMORE, MD 21203

1590Z/KP:jms/840306

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CCD
Charge Coupled Device
High Speed Sampling
Analog Buffer

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This Final Report describes the design, construction and operation of a 80-stage, high speed CCD based Bandwidth Compression Module which samples a high speed signal at 400MHz, stores this data, and reads the data out at a 400KHz rate. The module is to be used for laser pulse recording.

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TABLE OF CONTENTS

APPENDIX
(OPERATING MANUAL)

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1.0 SUMMARY

This report describes the design and construction of a CCD based transient recording unit nereafter referred to as the Bandwidth Compression Module (BCM). This module has been delivered and has been demonstrated at a sampling rate of 550 MHz.

1.1 Application Background

The Amphibious Warfare group at the Naval Coastal Systems Center in Panama City, Florida, had begun investigating the use of a blue green laser system for ranging in coastal waters. Specific applications include the preparation of charts showing water depth accurate to within one foot. Acoustic measurements are very time consuming to accomplish this function. An aircraft with a laser ranger could perform this function in a fraction of the time required by a surface ship. The measured depth would be proportional to the time difference between surface reflection and bottom return. This system is represented in Figure 1.

The signal processing of the laser return is a difficult problem due to the very narrow laser pulse (5-10nsec.) and the extremely fine time resolution (~2nsec.) required to obtain 1 ft. range resolution. The problem would be simplified considerally by recording the laser pulse and playing the recorded data back at a slower rate for ease of processing. This can be accomplished in a high speed Charge Coupled Device which samples and stores the data at a high rate and then clocks the data out at a slow rate.

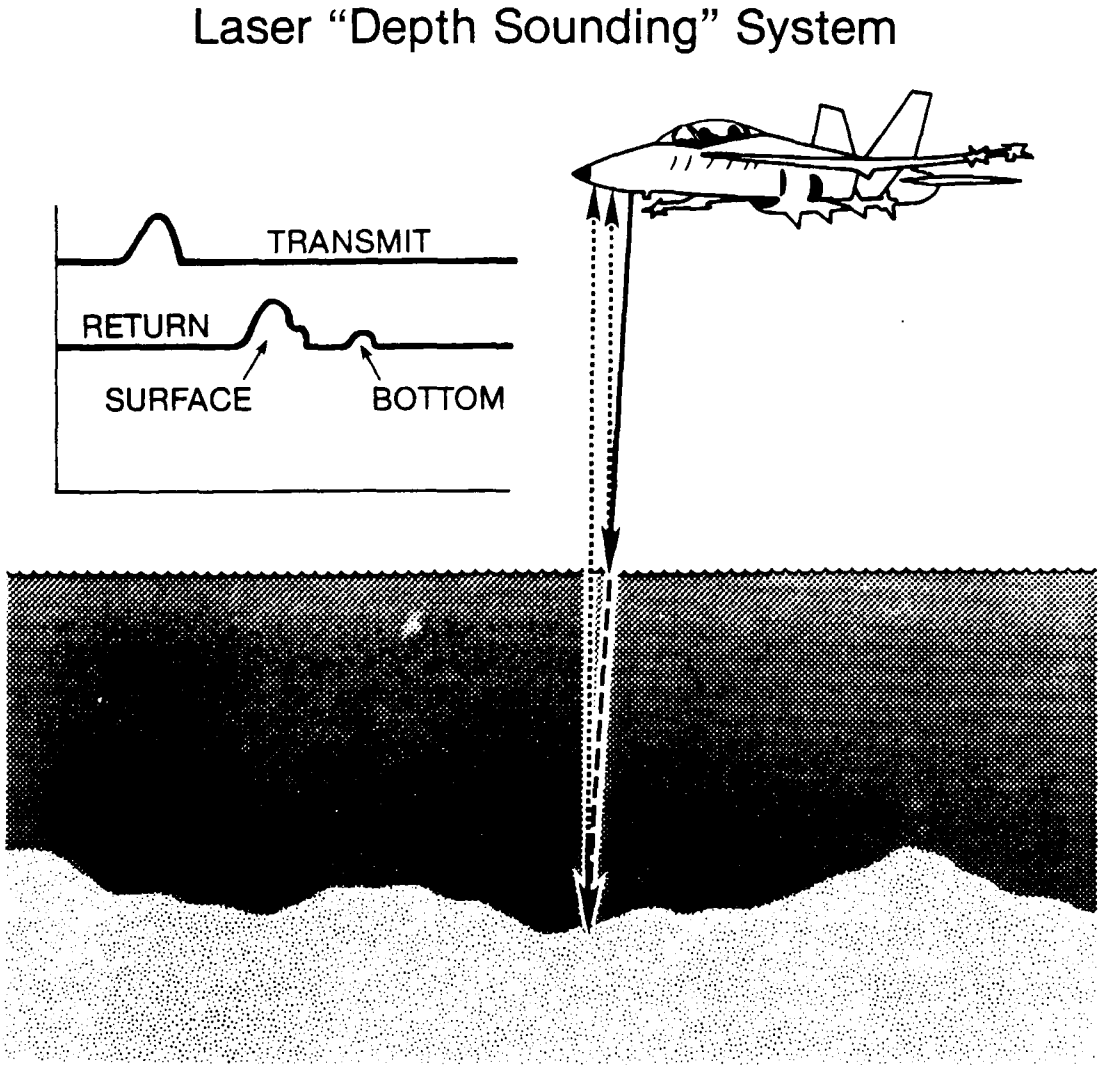
Laser "Depth Sounding" System
TRANSMIT
RETURN
SURFACE
BOTTOM

FIGURE 1

1.2 Goals and Objectives

The object of this program was to design and deliver a BCM to the Naval Coastal Systems Center capable of time buffering a pulsed laser radiation return so that it could be operated on with a low cost, high resolution A/D converter. The laser pulses in question would appear in a 80 nsec. to 200 nsec. window and may possess information of a character that would make it desirable to sample them at a rate of every one to two nanoseconds. A dynamic range of 40 db is necessary to detect both ocean surface and ocean bottom returns.

The input signal would be in an analog form derived from a fast photomultiplier tube such as an RCA 8645. The output signal would also be an analog signal to be delivered to an A/D converter.

Deliverables on this program were the Bandwidth Compression Module, a spare high speed hybrid containing high speed ECL logic, phase drivers and CCD device, and operating instructions.

2.0 TECHNICAL DISCUSSION

This section describes some of the design considerations investigated during the design and development of the BCM. Included are sections describing CCD architecture and preliminary testing. Since the operation manual went into detail on the construction and operation of the module, it will be included, less its appendix, as an attachment to this document to cover these points.

2.1 CCD Device

The original approach which was being pursued was the use of an 80 stage peristaltic CCD with a novel bipolar input structure. This device was included on the 7026 mask series which was being designed for another NRL program.

The bipolar input was essentially an NPN current mirror which injected charge into the CCD proportional to input voltage. A large emitter ratio made possible a low impedence input for high speed operation while injecting only a fraction of the input current into the CCD. Instead of using two isolated NPN transistors to realize the current mirror, a unique structure was designed to provide both a good physical coupling between the bipolar device and the CCD and to maximize the bandwidth of the current mirror. This structure never worked satisfactorily.

Another problem with this device was the integrating nature of the input structure. The charge injected into the CCD device with this input is proportional to the integral of the signal over one clock period. The transfer function of this "integrating filter" is:

$$H(f) = \text{SIN}\ (\pi f\tau)/(\pi f\tau)\ x\ e^{-j\pi f\tau}$$

If the input signal is half of the sample frequency, then the signal is attenuated 3.9 db. If a system with two such CCD's were used in a duplex mode where each CCD takes every other sample spaced 180^{o} apart, the sample rate would be twice the CCD clock rate, but the bandwidth is adversely affected by

the fact that the integration time is equal to the clock period, not the sample period. The duplex mode of operation is highly desirable since it makes sample ratio approaching 1GHZ in silicon feasable. This problem, which results in a null at the clock period, is shown in Figure 2. Because of both design problems and transfer function problems, no redesign of the 7026 mask was attempted and the bipolar input scheme was abandoned.

The fall back position was to use a partition mode device. An 80 stage partition device had been included on the 7019 chip set. Numerous devices were available and were packaged for use in the BCM.

Since the hybrid had been designed for the bipolar input, no seperate partition gate was available. To operate in the partition input mode, a partition driver had to be realized. The partition signal is normally a positive pulse timed so that both leading and trailing edges occur while the first phase gate (ϕ_1) is repulsive (low voltage state). To remedy this problem, non overlapping phase clocks were produced by careful adjustment of the numerous bias voltages associated with the driver (schematic appears in the attachment), and the $\phi 2$ signal was used for the partition gate.

A cross section of the CCD device used is included in the operating manual.

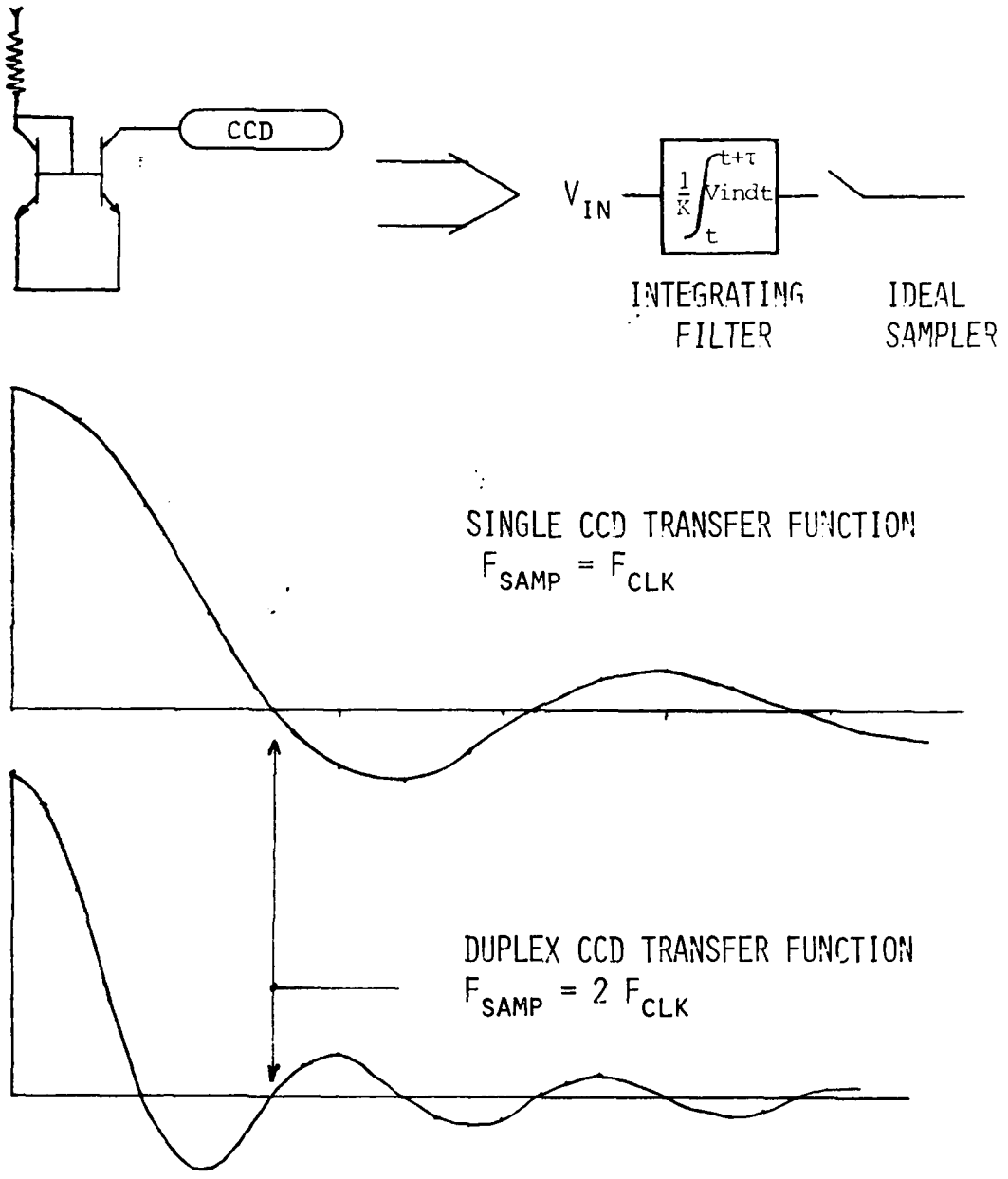

FIGURE 2 - TRANSFER CHARACTERISTICS OF THE BIPOLAR INPUT

2.2 Detailed Design, Construction, and Operation

(See Attachment.)

2.3 Test Results

Late in 1982 devices were found with acceptable but not ideal operating characteristics. However, since the devices worked at more than 400 MHZ there was a reluctance to remove it from the hybrid and replace it with another device which may or may not operate. The fear of Murphy's laws prevailed and this original device was left in the unit. All subsequent tests using an A/D converter and digital analysis were performed on this device.

When the laser lab at NCSC neared completion and del ry of the unit was desired, the spare hybrid was assembled and another ice was found. This device proved to be much better than the original device armed with a working spare the original device was replaced and a second better device was inserted. However the impending delivery and non availability of our digital acquisition system prevented further testing.

The difference between the old device and new device can be seen in Figure 3. From these pictures a marked improvement in performance can be seen, both in dynamic range and transfer efficiency.

Dynamic range measurements via spectral analysis made on the original device are attached in Figure 4. This data indicated a dynamic range of 30 db. Since the 128 point real FFT used a hamming window on the 80 samples and zero filled the remaining 48 samples, the noise bandwidth is approximately

(.075 F_{SAMPLE}) so 11.3 db must be added to the FFT S/N to obtain signal to RMS noise ratio. Measured values showed a max signal to noise floor of approximately 40 db, which translates to 28.7 db dynamic range for the original device. Comparing the pictures in Figure 3 indicate much better dynamic range, probably approaching 40 db, for the new devices.

Although all test data and pictures of the output were made with an input sample frequency of 400MHz, 550MHz operation was demonstrated during delivery, and NCSC indicated that the unit would probably be operated at 500MHz during system evaluation.

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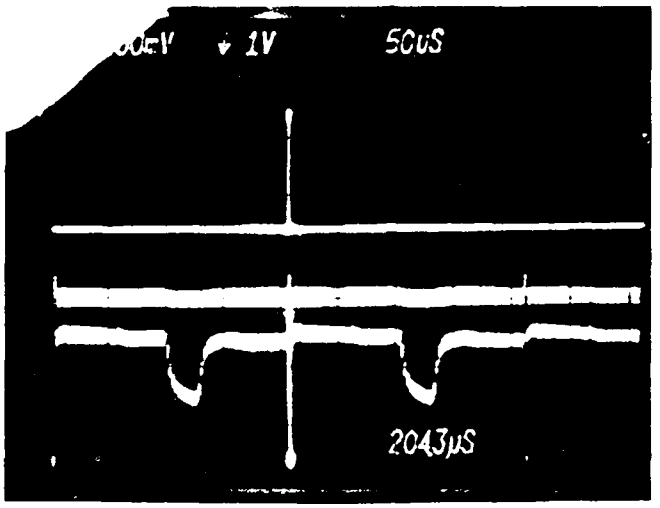
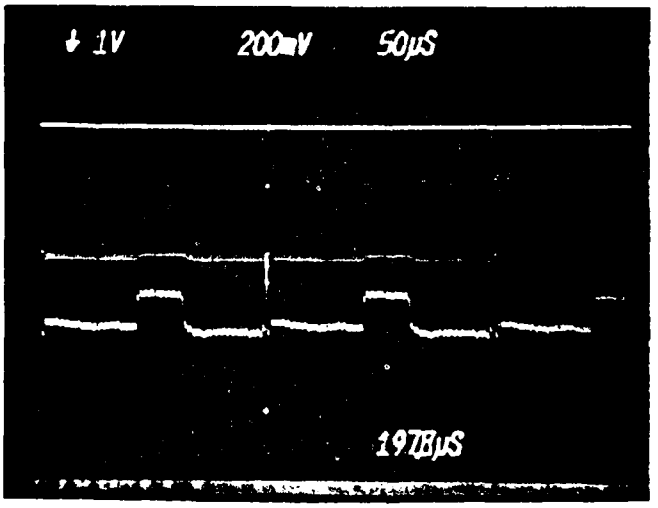
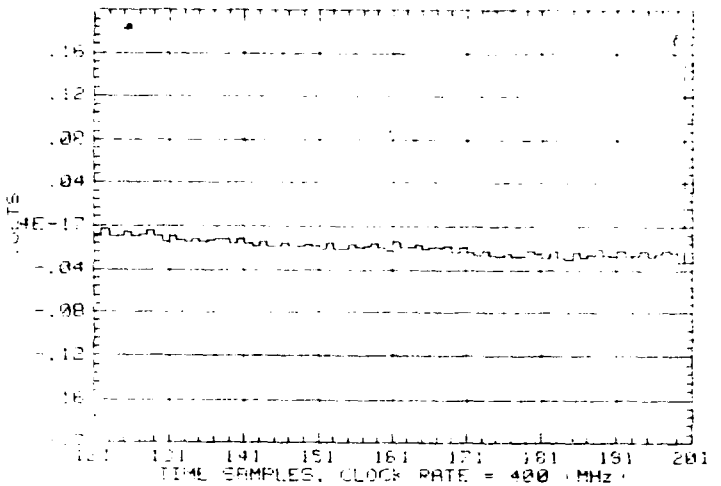


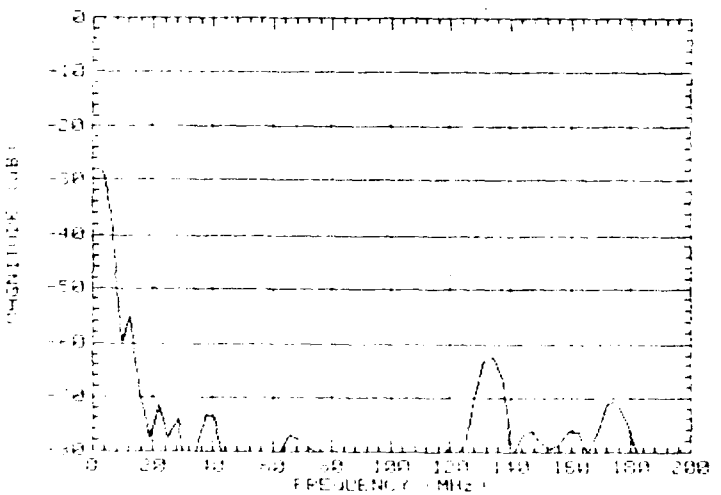
ORIGINAL DEVICE



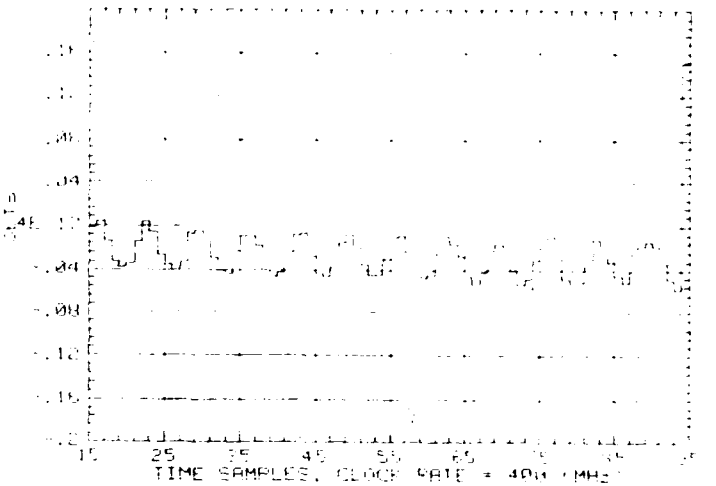
DELIVERED DEVICE

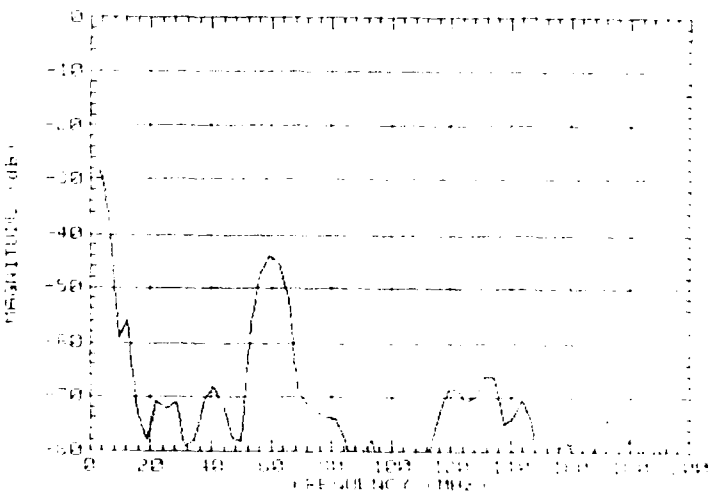
FIGURE 3 - COMPARISON OF TESTED AND DELIVERED DEVICES





FIXED PATTERN NOISE





SIGNAL INPUT AT
MAX AMPLITUDE - 2.5 DB.

FIGURE 4 - TEST DATA (AMPLITUDE SCALES ARE NOT CORRECT)

** APPENDIX **

This attachment consists of the operating manual delivered with the unit without the operating manual's appendix, which consisted of detailed construction sketches.

1.0 DESCRIPTION

1.1 GENERAL INFORMATION

The Electronic Bandwidth Compression module is an experimental subsystem which will sample a video signal at a high input rate (~ 400MHz), store 80 such samples, and read these samples out at a baud rate 1000 times slower than the input frequency. This system was originally designed around a 7026 bipolar input device. This device was never satisfactorily fabricated, and the system was modified to utilize an 80-stage 7019 partition mode device. Although operation of this two phase device ideally requires a special partition gate driver, one of the phases was used which produced proper operation. Adjustments are, however, somewhat critical since the driver circuitry must be adjusted to produce non-overlapping clocks.

1.2 CCD DEVICE DESCRIPTION

The 7019 80 stage device used in this module is a two phase buried channel CCD. The electrode structure consists of 4μ polysilicon gates which form both the holding well and the self aligned mask for the P implant to produce the potential step necessary for two phase operation. This implanted region is then covered by an aluminum gate and electrically connected to the adjacent holding well. A cross section of the CCD structure is shown in Figure 1.1. This figure also shows how each bias potential is connected and is an excellent reference diagram to use when adjusting the numerous bias voltages.

1.3 THEORY OF OPERATION

The operation of the Bandwidth Compression Module is very similar to that of a transient recorder. In the standby or dormant mode of operation, the clocks will be operating in the fast mode with the CCD always sampling input data. Data taken during this mode are shifted through the CCD at the fast clock rate and simply dumped at the output by keeping the reset transistor on. Upon application of a start pulse, logic is initiated which starts a slow output mode after 80 counts. Slow output then commences, with the analog output of the CCD being routed to the output connector. The analog sampled data appears at the output with an output rate 1/1000th of the sample rate.

The CCD itself samples the input signal using a partition mode input. In this method of charge injection, a charge proportional to the difference between the input diode potential and the signal potential resides in the area under electrode G3. A partition gate is then pulsed to a low potential isolating this charge and allowing injection into the CCD.

1.4 PHYSICAL DESCRIPTION

The electronics for this unit are assembled in a 19"x8 3/4"x17" deep rack mountable assembly. All inputs and outputs are applied via BNC connectors on the front panels. These signals are described in Table 1.1 and are further defined elsewhere in this manual.

There are numerous potentiometer adjustments which appear on the front panel. These adjustments control variable power supplies and variable regulators for both power and bias voltages. These potentiometers and the voltages controlled are listed in Table 1.2. A switch and test points to monitor the various voltages are also present to aid in adjustment.

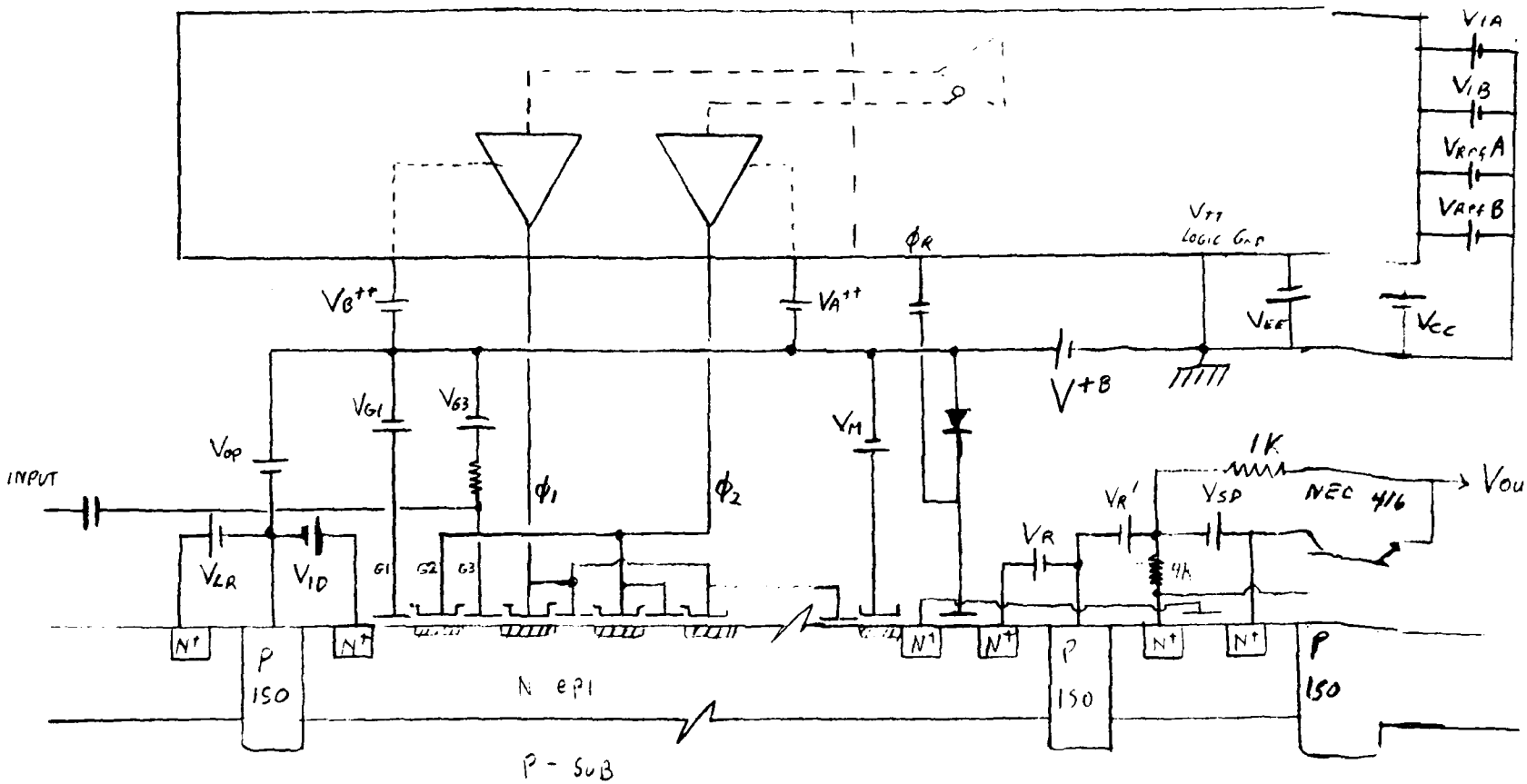


FIGURE 1.1
CCD CROSS SECTION SHOWING
BIAS VOLTAGE AND CLOCK CONNECTIONS

TABLE 1.1

I/O SIGNALS

Signal Name	Description
Clock In	400 MHZ master clock equal to sample frequency. Amplitude ~1v P-P into 50Ω. Amplitude adjustment critical for proper logic operation.
Range Gate	ECL compatible start command. Normally high (~1v). Sample cycle starts on high to low transition. Leaving input disconnected forces module in auto cycle mode.
Data	ECL output synchronized with analog output for A/D strobe.
SYNC	ECL output used for synchronization in auto cycle mode.
Fast/Slow Clock	SYNC - Needs 50Ω load.
Bin	Analog input - 50Ω
Bout	Analog Output - 1KΩ Termination*
Ain/Aout	Not used - For further expansion.

*Because of high output offset voltage (~ 8V PC), a low impedance termination would cause failure of the output transistor due to excessive currents. See Figure 1.1 for schematic.

TABLE 1.2

POTENTIOMETER ADJUSTMENTS

Potentiometer	Description of Controlled Signal	Voltage Range Referenced to Chassis
V_{EE}	ECL Logic Pwr V_{EE}	Set -3 to -6
V_{TT}	ECL Logic Pwr V_{CL}	Set +2 to +3
V_{1A}	Diff Amp A Neg. Pwr.	0 to -10
V_{1B}	Diff Amp B Neg. Pwr.	0 to -10
$V_{REF}A$	Positive Ref - Input Side of AmpA	0 to +10
$V_{REF}B$	Positive Ref - Input Side of AmpB	0 to +10
$V^{+}A$	Not Connected - $V^{+}B$ used	
$V^{+}B$	Positive Ref for Output Side of Predriver - Source of GaAS FET	0 to 10 Limits @ Pot Center
$V^{++}A$	Positive Driver Load Voltage	(0 to 20) + $V^{+}B$
$V^{++}B$	Positive Driver Load Voltage	(0 to 20) + $V^{+}B$
V_{OP}	Substrate Bias with Respect to Lower Clock	$V^{+}B$ - (0 to 24v)
V_{R}	CCD Reset Voltage	(0 to 20v) - $V_{OP}+V^{+}B$
V_{R} 1	Load Resistor Reference for Output Follower	(0 to 20) - $V_{OP}+V^{+}B$
V_{LR}	Leakage Ring Around CCD	(0 to 24) - $V_{OP}+V^{+}B$
V_{SD}	Drain Voltage for Output Follower	(0 to 24) + $V_{OP}+V^{+}B+V_{r}'$
G1	1st CCD Gate	(0 to 24) + $V^{+}B$
G2	Output Shield Voltage	(0 to 24) + $V^{+}B$
G3	Input Fat Zero	(0 to 20) + $V^{+}B$
V_{ID}	Input Diode	(0 to 12) + $V^{+}B-V_{OP}$
V_{M}	Output DC MUX	(0 to 24) + $V^{+}B$
V_{COL}	Lower Clamp for Φ_{R}	(0 to 24) + $V^{+}B$

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2.0 SUBASSEMBLIES

2.1 POWER DISTRIBUTION AND BIASING

There are ten small power supplies which supply power and bias levels to the module circuitry. Main power is supplied to the drawer through the main power switch on the front panel. PS2 through PS10 have individual AC power switches so that parts of the circuitry can be inhibited for test or checkout. This wiring is shown in Figure 2.1.

All voltages associated with the high speed drivers originate in power supplies PS1 through PS5, and are regulated by variable regulators mounted in the chassis. The scheme is shown in Figure 2.2. Although a potentiometer control exists to vary $V^{+}A$, this potential is not used in the circuitry. A detailed wiring diagram of each regulator is shown in Figure 2.3.

Bias voltage to the CCD which require little current are produced in PS6 through PS10 and are adjusted by potentiometers on the front panel. These connections are shown in Figures 2.4 and 2.5.

2.2 ELECTRONIC CIRCUITRY

The central electronic component containing both logic and analog circuitry is a composite module consisting of a wire wrap board modified to accept a large power hybrid. The wire wrap board contains lower speed ECl logic while the hybrid contains all high speed (> 100 MHZ) logic, translators, and GaAS phase drivers.

2.2.1 LOGIC

The logic diagram which includes the circuitry for both high and low speed logic sections is shown in Figure 2.6. A clock input equal to the sample frequency, which is applied to a PNC on the front panel and routed to the hybrid through a small SMA jumper, is AC coupled to the logic threshold (A1U1), and applied to the circuitry. In the standby mode of operation, this signal is gated through A1U2 and applied to the drivers to generate the clock phases. Both the high speed counter (A1U5, A1U6, U15, U10, U4) and the low speed output counter (A1U3, U6, U7, U2, U8, U9) are held off in this state.

Upon application of a range gate start pulse, flags are set which initiate both fast and slow counter chains. When the fast counter chain reaches a count of 80 (U4 Q2 low to high transition) the high speed clock signal is gated off and the slow clock phases are routed to the drivers. When terminal count is reached (U9) the counters are reset and the system goes back to the standby mode.

The ECL logic operates from a floating power supply with V_{TT} tied to ground (chassis). This grounding scheme enables the operator to use positive voltages referenced to chassis in system operation.

A logic diagram showing the critical waveforms appears in Figure 2.7.

2.2.2 CLOCK DRIVER

A schematic of the clock driver circuitry is shown in Figure 2.8. Two copies of this circuit are included within the hybrid.

Each phase from the ECL logic is first buffered in an ECL inverter to create a complementary output. This output is then amplified in a differential amplifier made up of NE219 chip transistor. An NE416 transistor

with 20Ω emitter resistor make up the active current source. All voltages applied to the differential amplifier are controlled separately via front panel adjustments. The $V^{+}B$ voltage is common to both drivers and provide a baseline reference voltage for CCD operation.

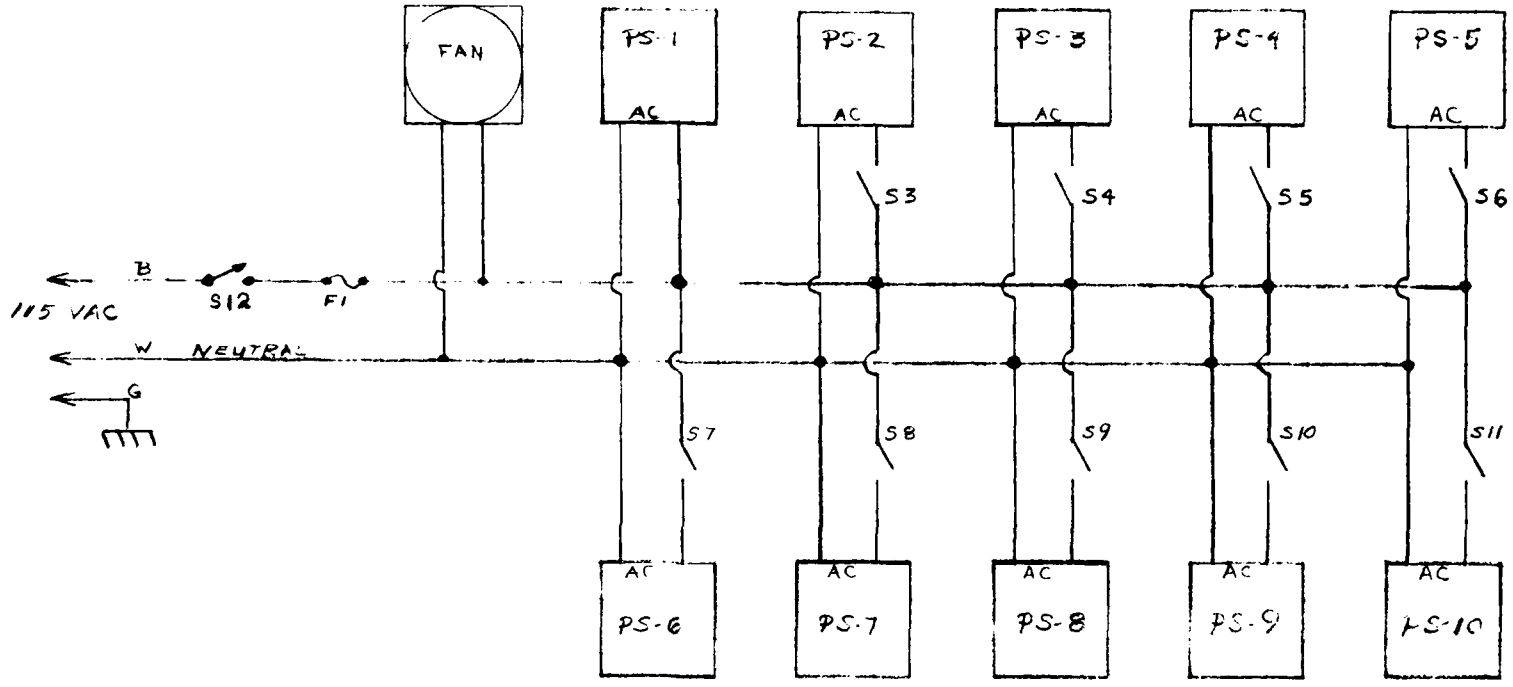
The final driver stages use MSC88002 GaAs FET power transistors with a 50Ω pull up resistor in a common source stage. This device is positioned very close to the CCD, minimizing inductance effects.

2.2.3 PACKAGING

The overall layout of the mother board is shown in Figure 2.9.

Modifications were made to the mother board to allow the hybrid to plug into sockets U16, 21, 26, 20, 25, and 30 of the mother board. Signal names are referenced on the layout.

The hybrid circuit contains various hybrid substrates mounted in the same package. The high speed logic is contained on a 1" x 5/8" substrate, the predrivers are mounted on 1/4" x 1/4" substrates, and the CCD and associated circuitry are mounted on a third substrate. The GaAs FETS and 50Ω power resistors are mounted directly to the package bottom for heat dissipation. A picture of the hybrid with the various circuit functions is attached in Figure 2.10. The CCD itself is packaged in a 24 pin flatpack and soldered to the CCD substrate. Input and output circuitry indicated in Figure 1.1 is also mounted on the CCD substrate. Additional bonding information can be found in the appendix.

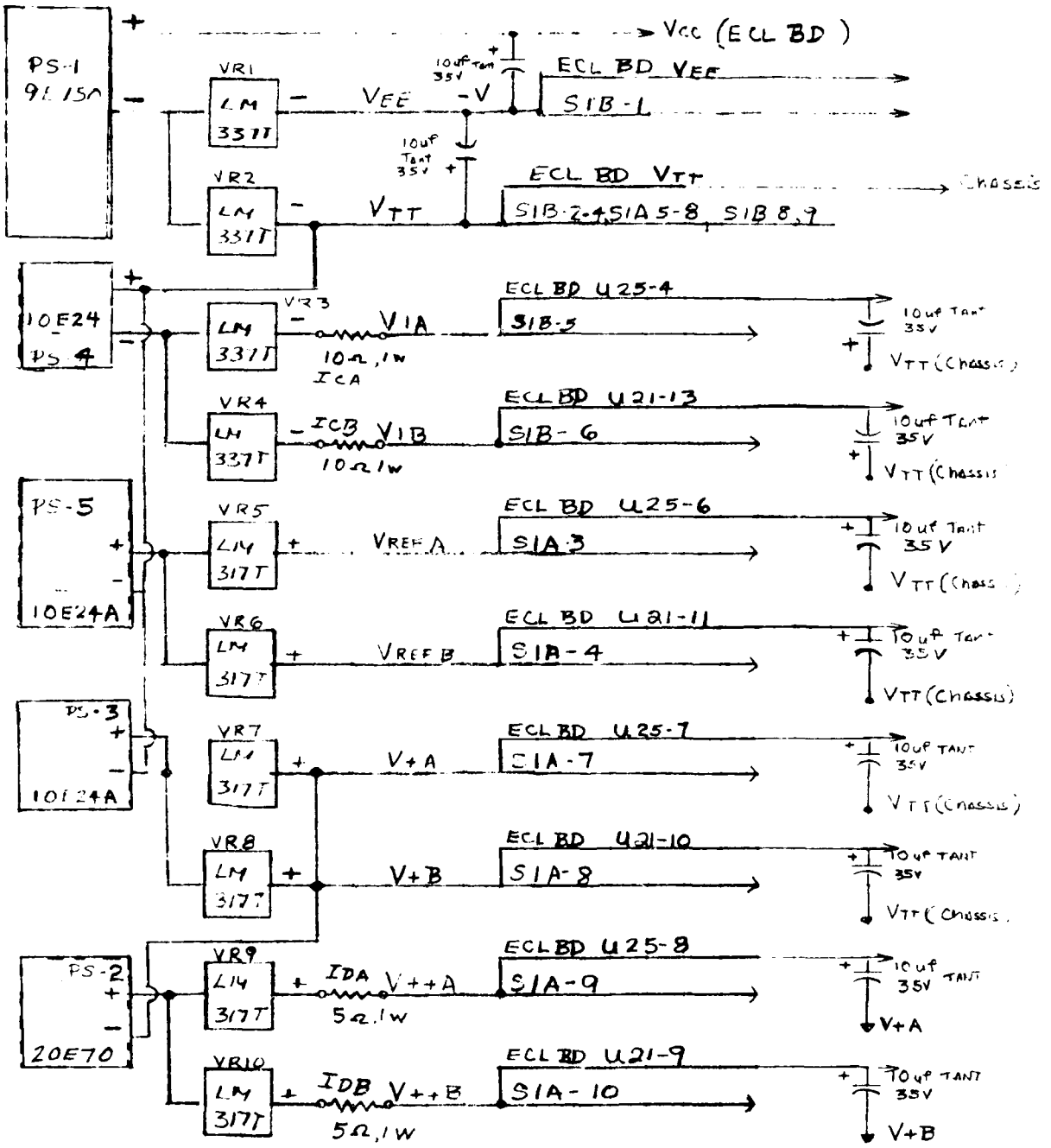


Symbol	Acopian Model No.
PS-1	9E150
PS-2	20E70
PS-3	10E24A
PS-4	10E24A
PS-5	10E24A
PS-6	24E10A
PS-7	20E06
PS-8	20E06
PS-9	20E06
PS-10	20E06

AC WIRING DIAGRAM
FICSC EBCM

FIGURE 2.1

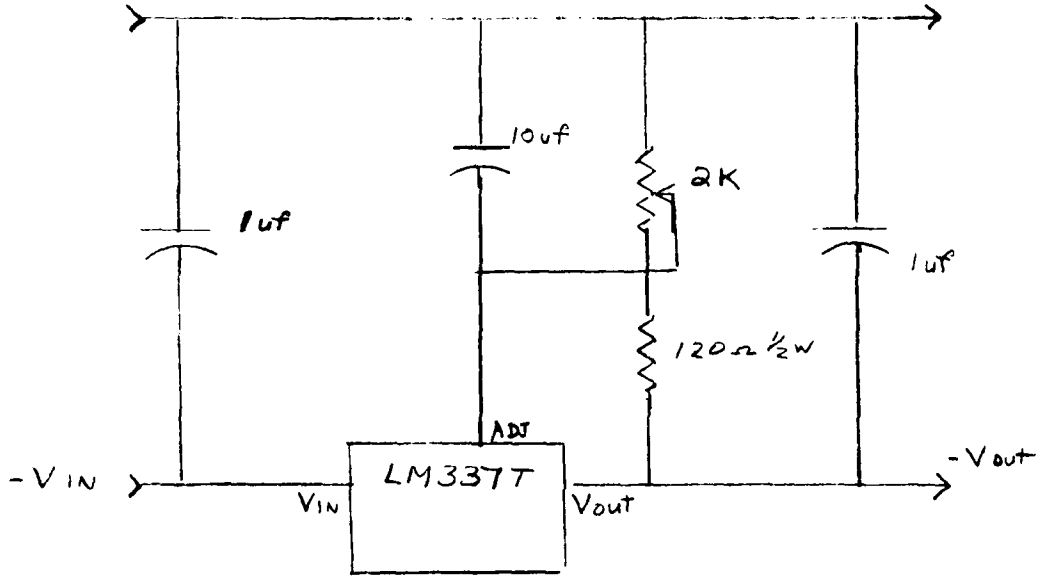
Regulator Wiring Diagram NCSC **EBCM**



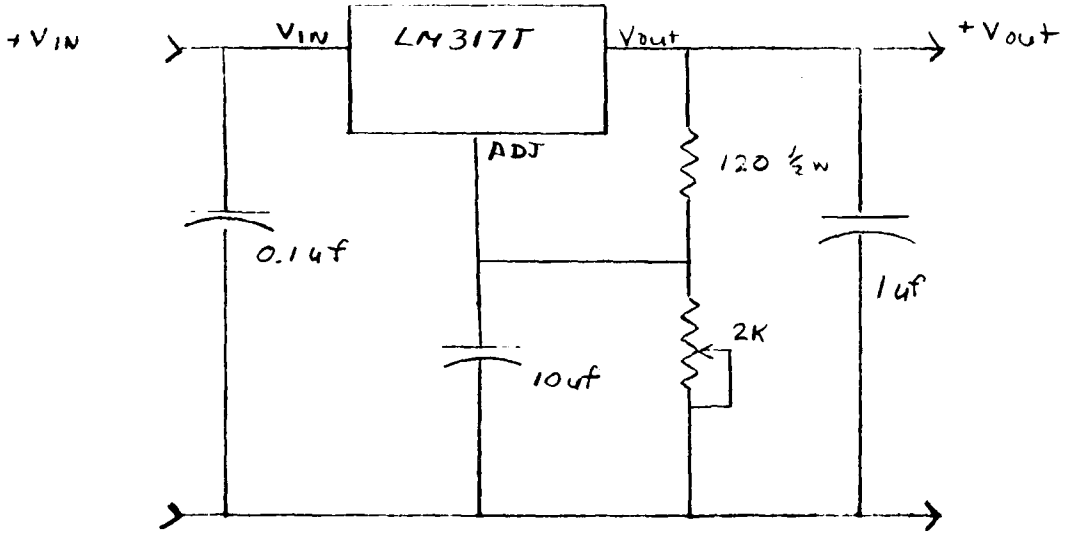
NOTE: $V^{+}A$ IS NOT ACTIVE

FIGURE 2.2

Regulators NCSC EBCM



VEE
VTT
VIA, IB



VREF A
VREF B
V+ A
V+ B
V++ A
V++ B

All capacitors are tantulum

FIGURE 2.3

NCSC - EBCM DC POWER DISTR.

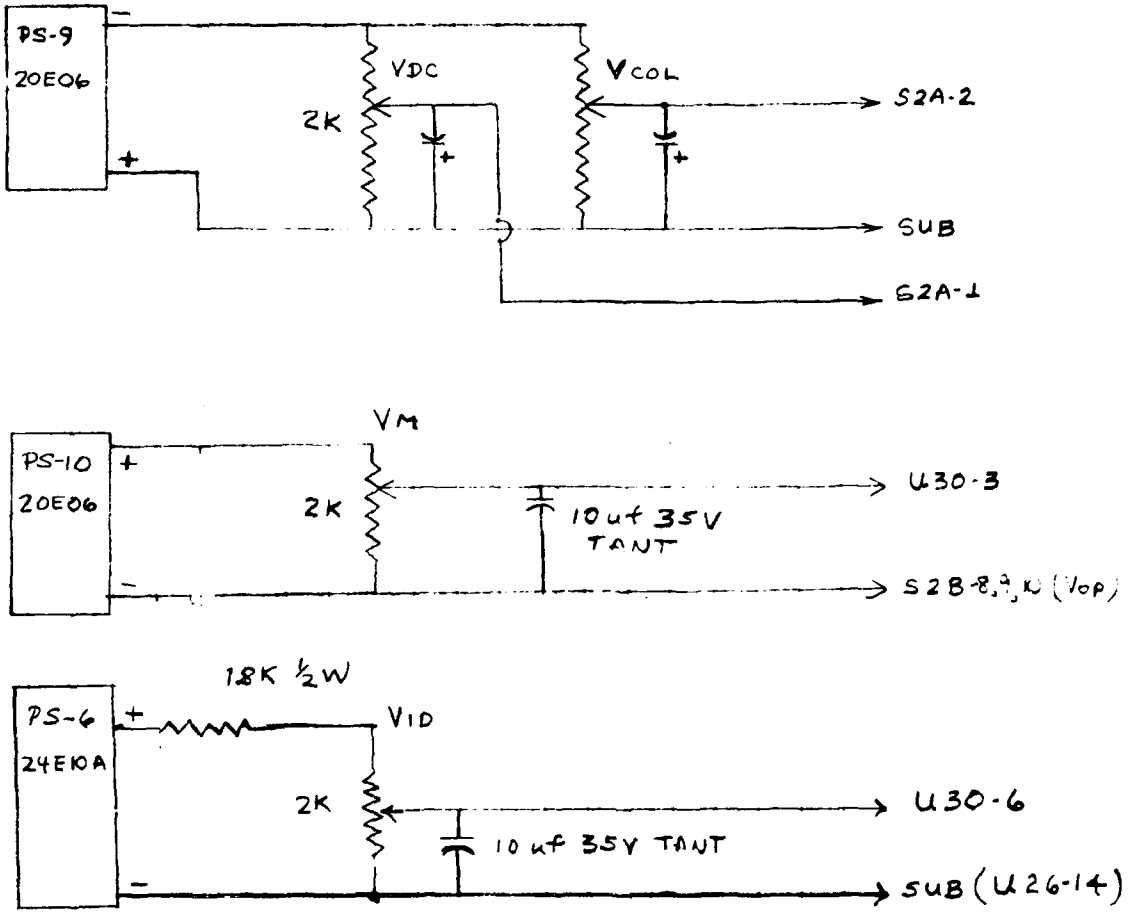


FIGURE 2.4

NCSC EBCM DC POWER DISTR

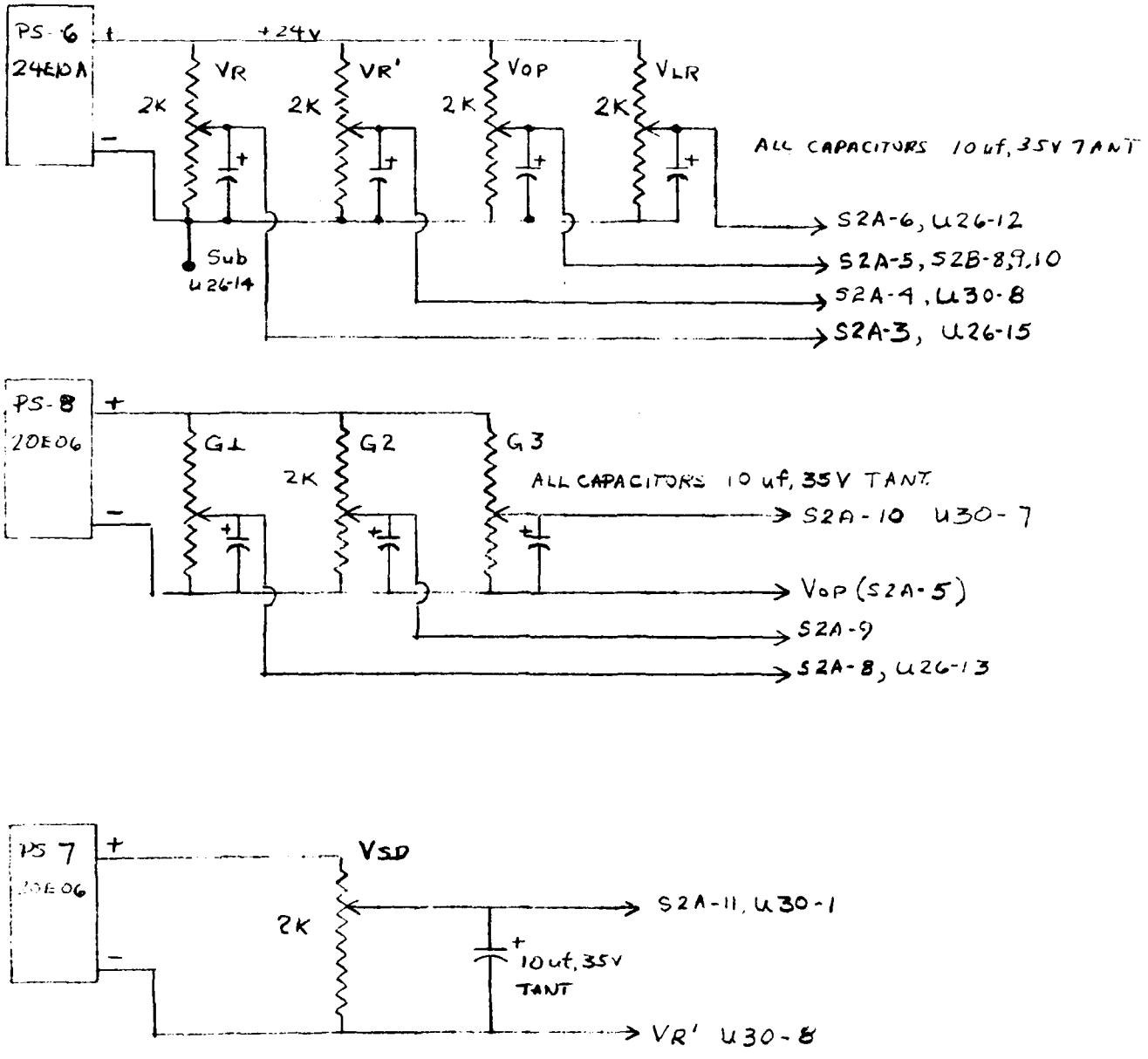


FIGURE 2.5

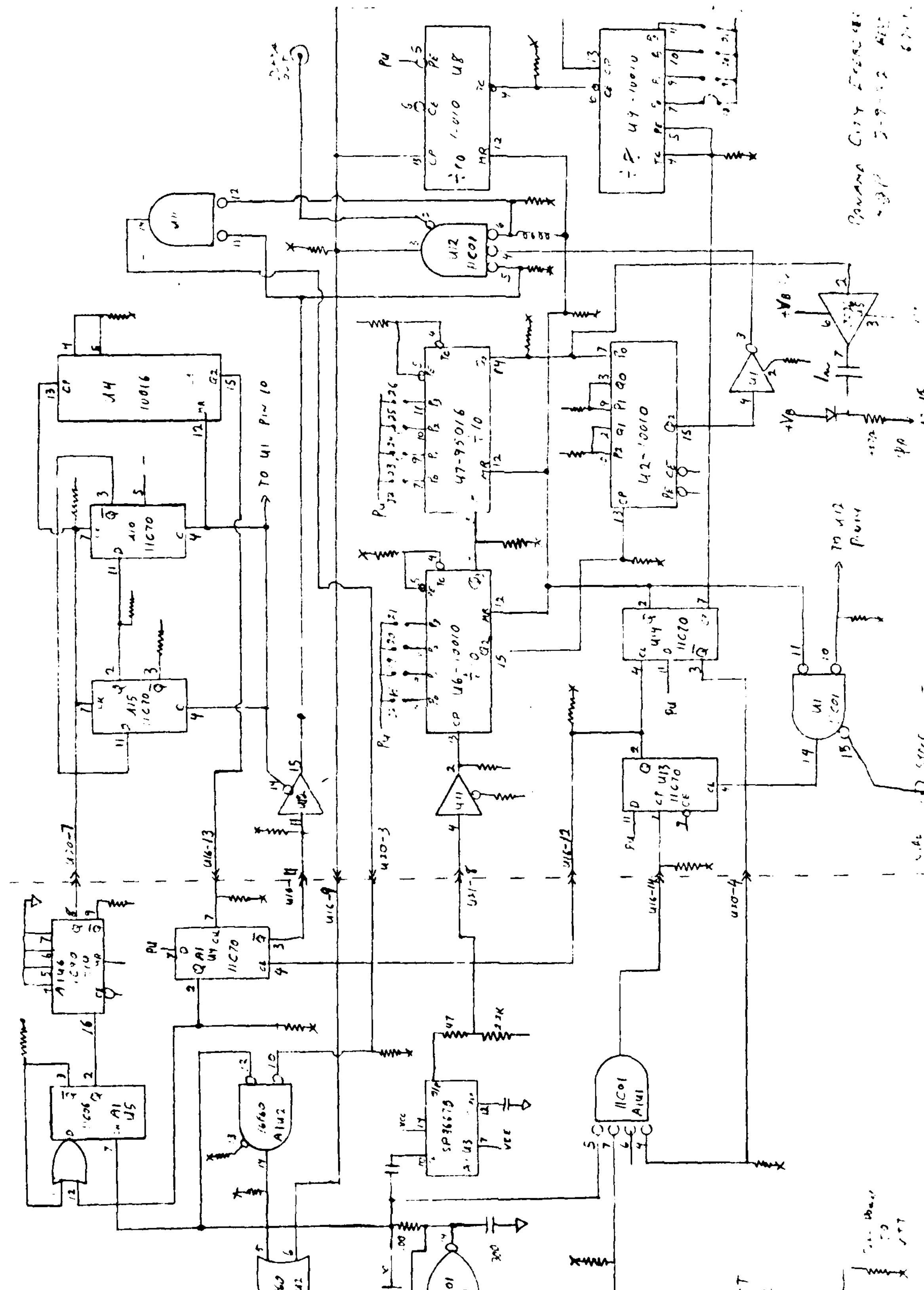
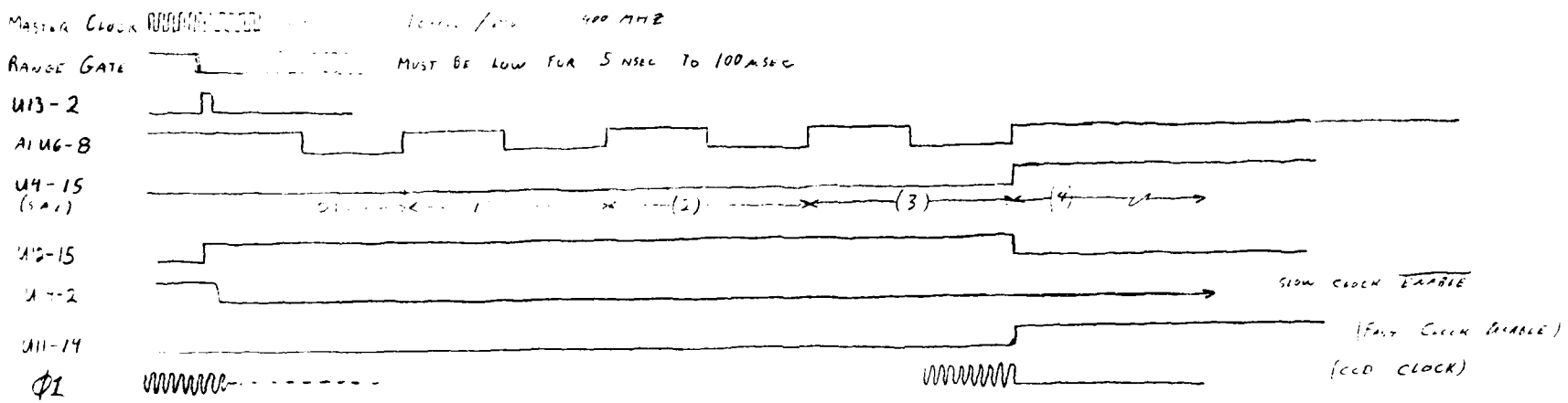
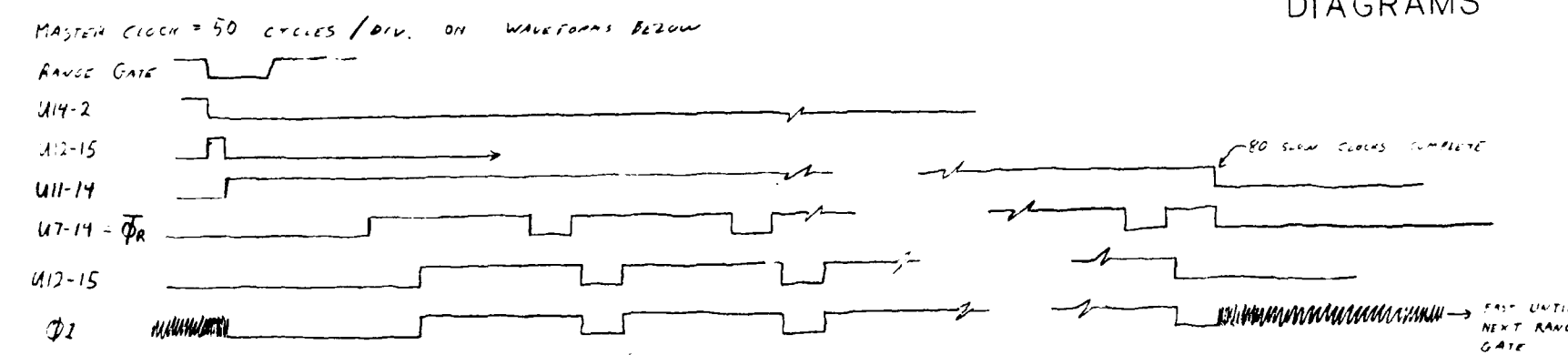


FIGURE 2.6



FAST/SLOW TIMING

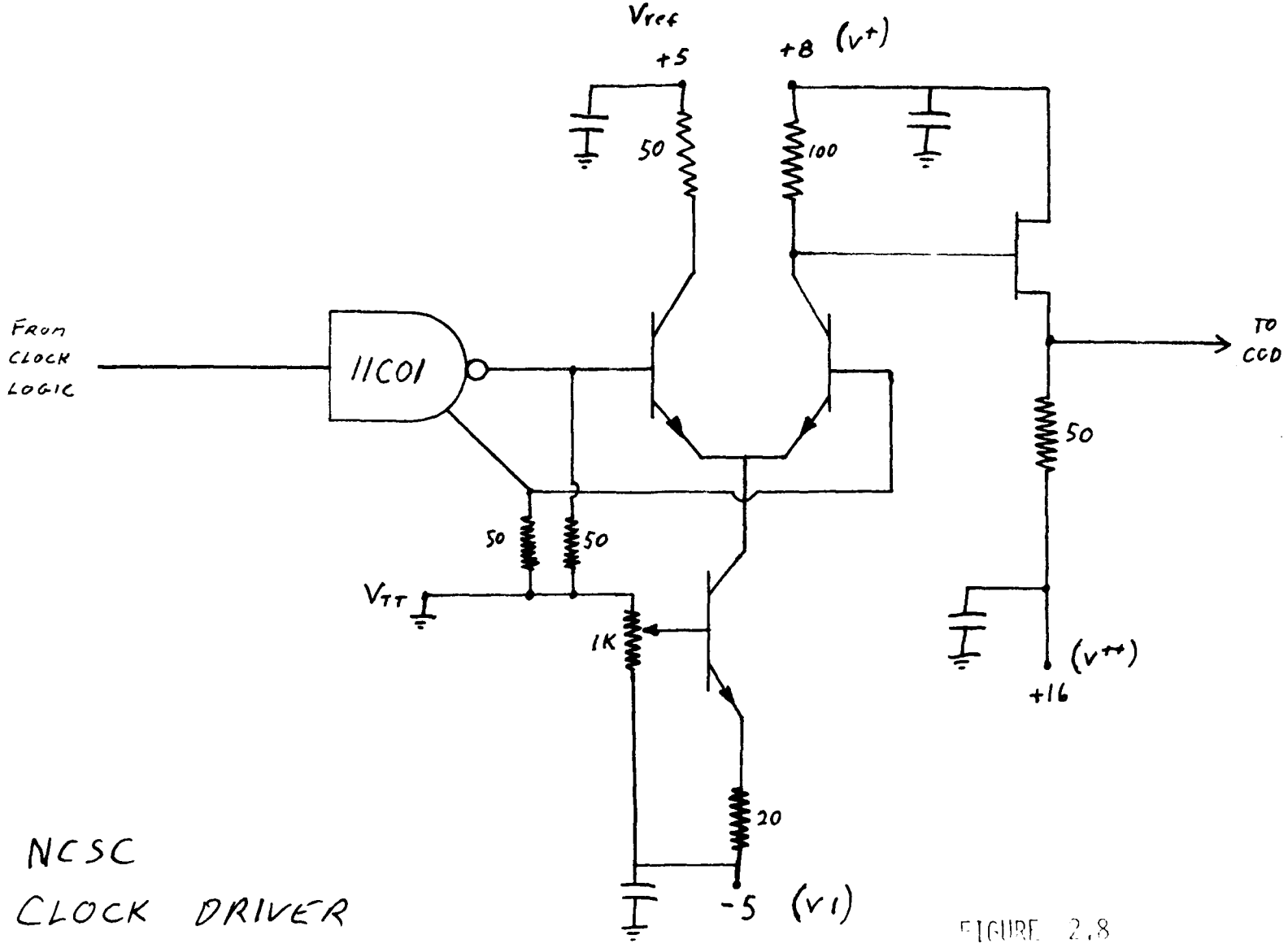
TIMING DIAGRAMS



SLOW CLOCK GENERATION

FIGURE 2.7

REVISED
A 2P 5/21/+



NCSC
CLOCK DRIVER

FIGURE 2.8

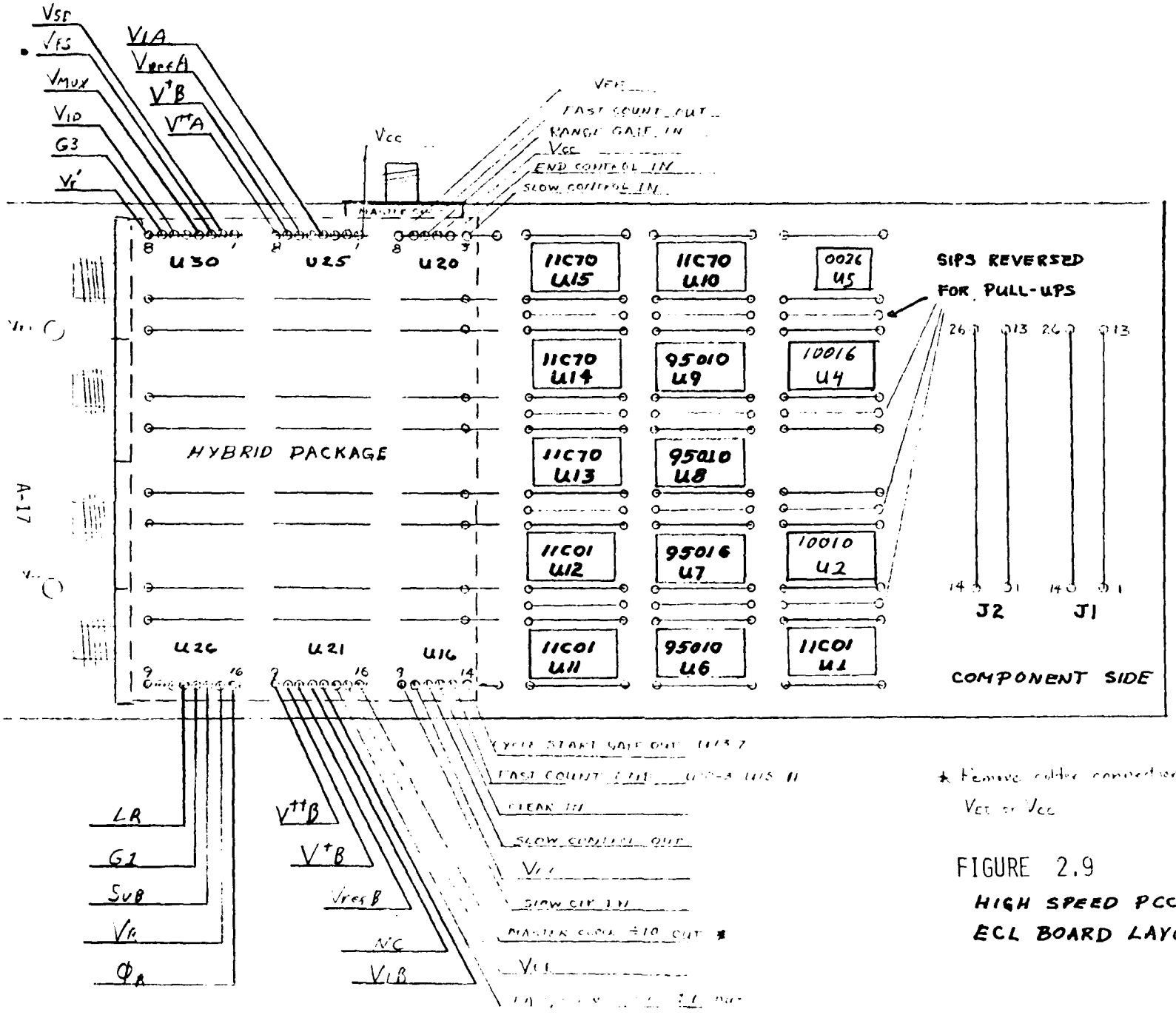
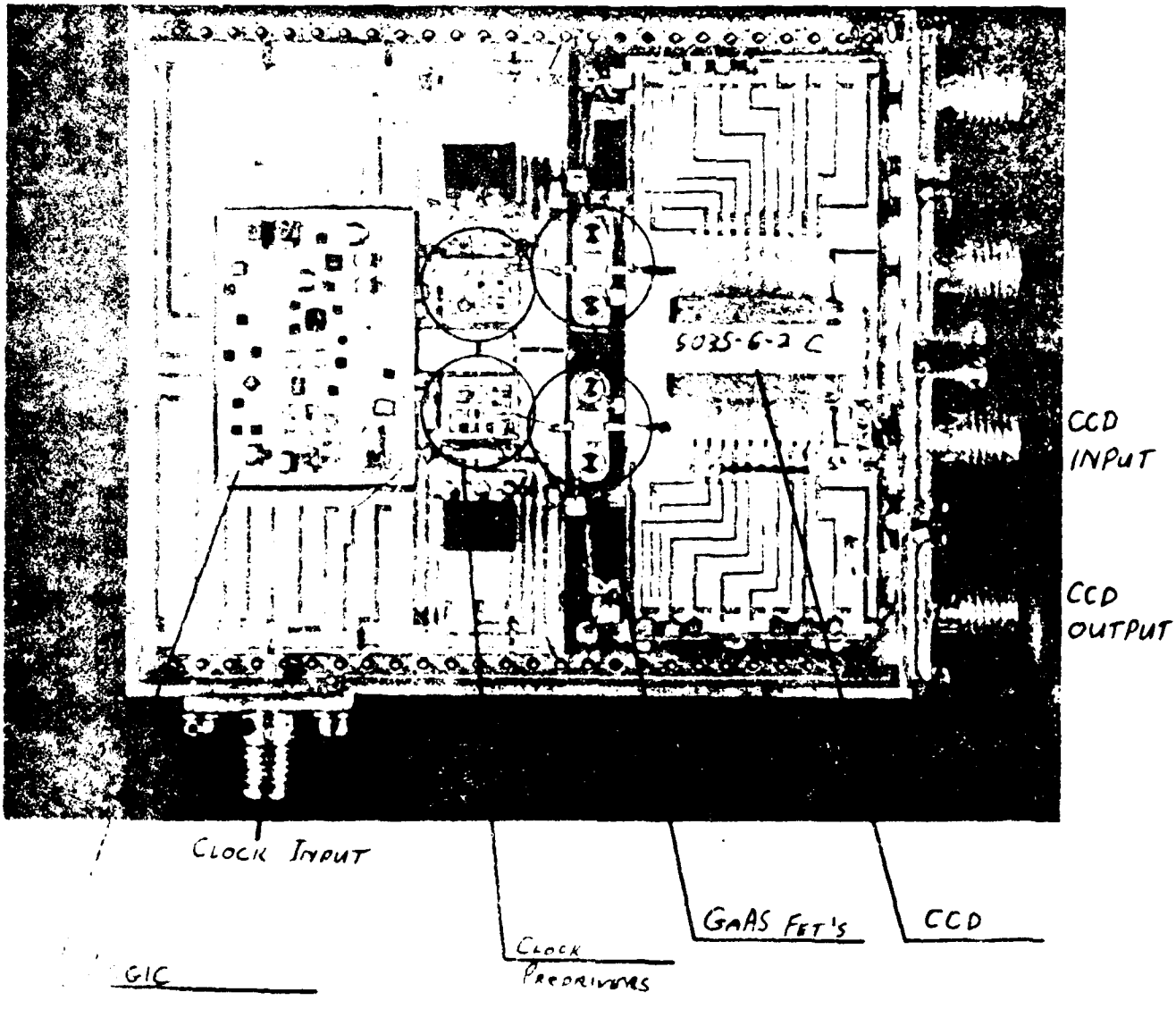


FIGURE 2.9
HIGH SPEED PCCD
ECL BOARD LAYOUT


5025-6-2 C
CCD INPUT
CCD OUTPUT
CLOCK INPUT
GIC
CLOCK PRODRIVERS
GaAS FET's
CCD

3.0 MODULE OPERATION

3.1 OPERATING CONFIGURATION

In order to utilize this subsystem in the bandwidth compression mode of operation, a trigger pulse must initiate the sample cycle, and some means must be provided to sample the analog output. Figure 3.1 shows a test configuration which was used for unit testing and provides the necessary elements for system operation. In actual operation the start pulse and the wide band input pulse would originate within the system to be sampled.

With no signal applied to this start pulse, the bandwidth compression module will go into a self trigger mode. In this mode the logic will continually cycle between 80 fast clocks and 80 slow clocks and is a useful mode of operation for troubleshooting purposes. There is a serious problem with this configuration which makes it marginally useful when setting up the CCD. During slow clock to fast clock transitions, transients associated with changing load requirements within the hybrid cause severe ringing which appears at the output as a fixed pattern noise and degraded CCD operation. A sufficient length of time permitting these transients to damp normally occurs during the standby or dormant mode of operation. Damping normally occurs within 100 fast clock cycles or 200 usec. If the self triggering mode is the preferred operating mode, the problem of transients could be corrected by moving the wire wrap connection going to U4 Pin 15 (Q2) to U4 Pin 14 (Q3). This will force the logic to produce 160 fast clocks to every 80 slow clocks allowing the 1st 80 slow clocks for transient damping.

Figure 3.2a shows the CCD operating in the self triggering mode with the logic rewired for 160 clock pulses. Figure 3.2b shows the normal mode of operation, with the input pulse at different positions within the sample window. Note the dead zone apparent in the output which corresponds to the standby or dormant period in the sampling cycle. Figure 3.3 shows the relationship between CCD output and data output, as well as the delayed pulse used as an A/D sample pulse.

3.2 ADJUSTMENT PROCEDURE

Because the ECl logic and the CCD is being operated at their high frequency limit, and driver matching is not ideal, many of the voltage adjustments are very critical and a few hundred millivolts of misadjustment can suppress all operation.

For ECL operation, V_{TT} and V_{EE} have been adjusted for satisfactory operation and should not require re-adjustments. The clock input is very critical at high frequencies, however, and requires some careful amplitude adjustments. If the clock amplitude is too low, the logic will not operate. As the clock voltage is increased, a very narrow range of voltages is encountered which produces proper logic operation. If the clock voltage is increased still further, a latchup condition will result which requires re-cycling the power switch.

To set the clock voltage leave the start pulse input disconnected to put the logic in the self trigger mode. Monitor the sync output of the unit on an oscilloscope with internal triggering. With a 400 MHZ input frequency increase the clock voltage until a steady pulse train with a 2 msec. period is noted.

To set up the CCD, start with the settings listed in Table 3.1. Using the test configuration shown in Figure 3.4, apply a pulse of approximately 2V P-P and 50 usec long to the analog input.

By adjusting the pulse delay, place the pulse within the sample window so that the sample output appears on the oscilloscope. Slight adjustments can now be made to the various driver voltages and CCD biases to obtain the most accurate pulse reproduction. The input clock amplitude may also require slight readjustment since only one ECL gate isolates the predriver from the ECL clock generation and its amplitude does effect the predriver. Operation of both hybrids delivered with the system when adjusted to the values in Table 3.1 is pictured in Figure 3.5.

The system is now ready for use and can be placed into an optical system.

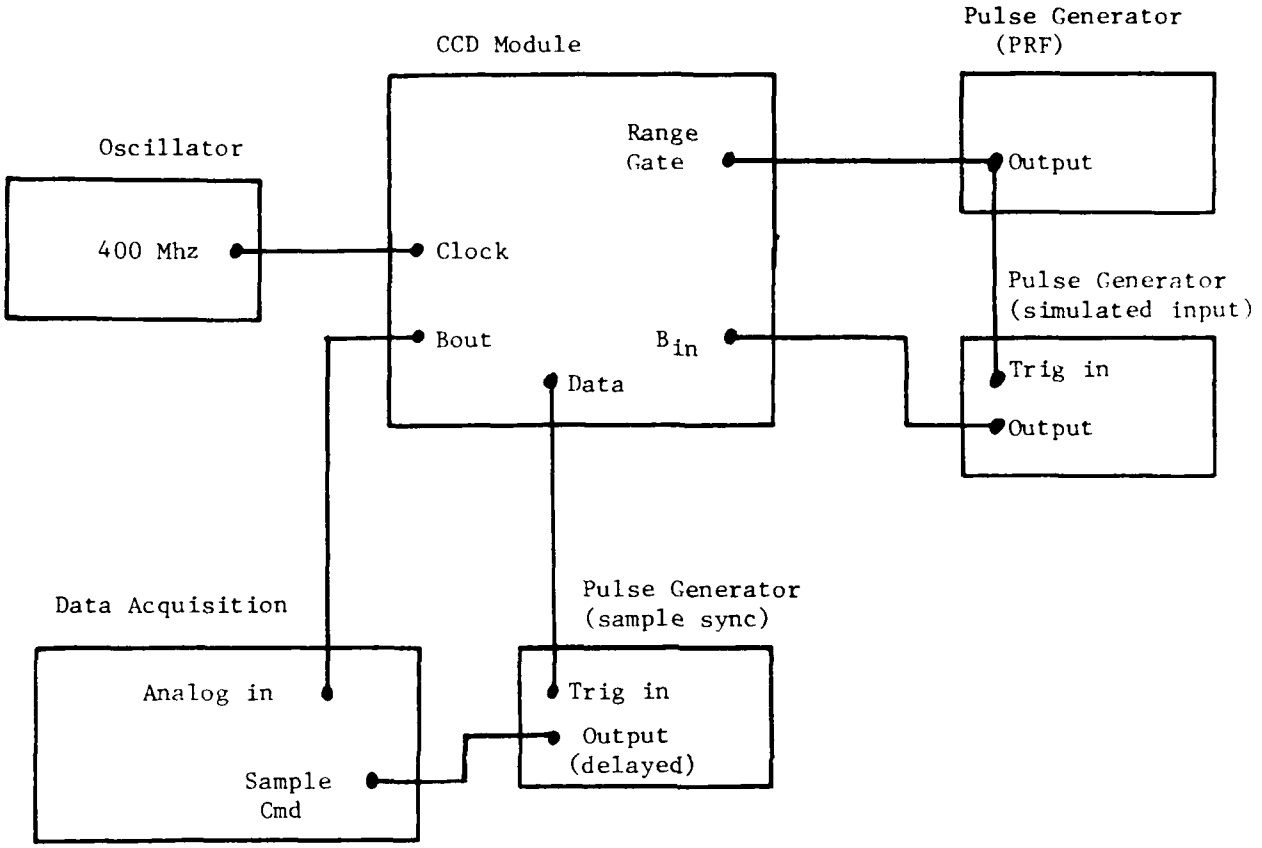
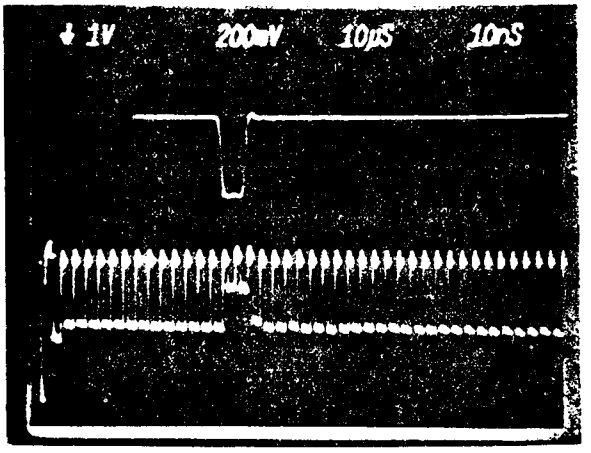


FIGURE 3.1

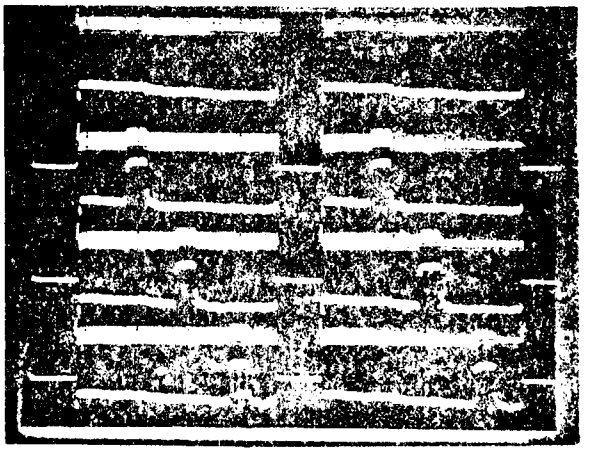
SYSTEM OPERATING CONFIGURATION



INPUT

(A)

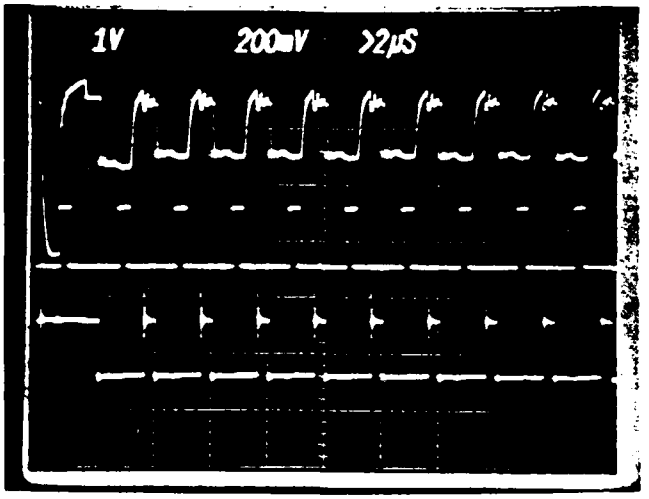
OUTPUT



(B)

FIGURE 5.3

TYPICAL ANALOG OUTPUTS



CCD OUTPUT

DELAYED SAMPLE PULSE

DATA FROM MODULE

FIGURE 3.3

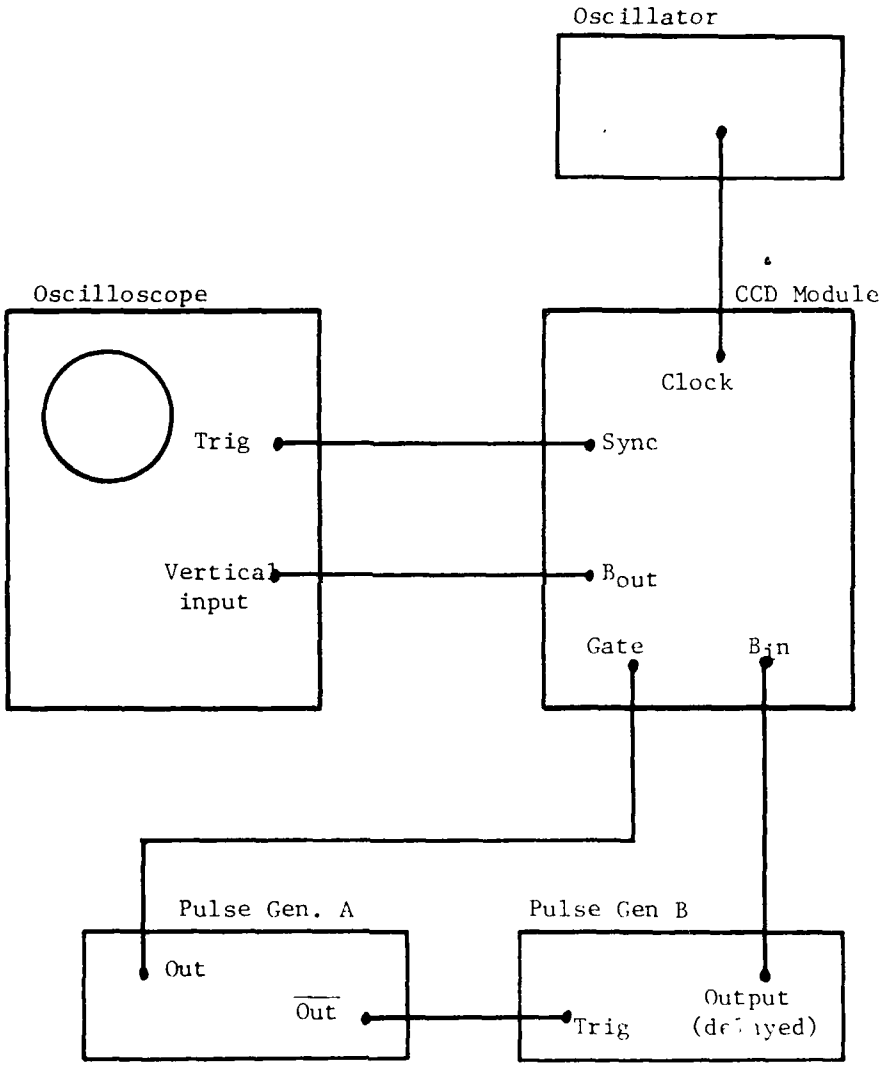


FIGURE 3.4

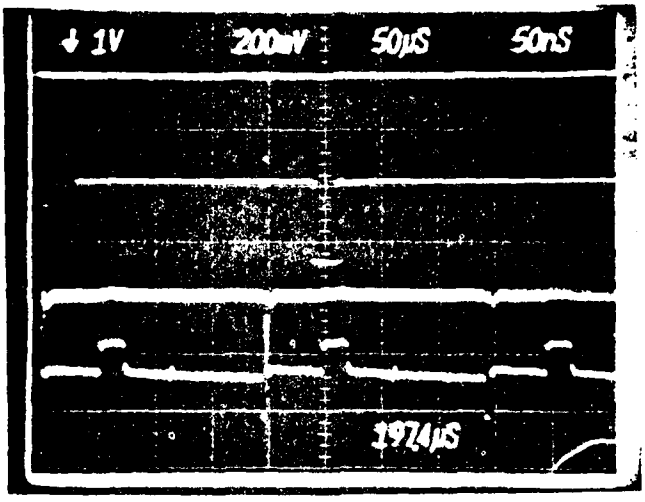
TEST CONFIGURATION

Trigger pulse generator B with Fast/Slow clock when in self trigger mode.

V_{EE}-815	V_{1A}-150	V_{REF} A-125	V^{+}A-NC	V^{++}A-640	G_1-510	V_{UD}-740
V_{TT}-65	V_{1B}-124	V_{REF} B-115	V^{+}B-355	V^{++}B-590	G_2-820	V_{M}-0
V_{R}-660	V_{R}-400	V_{OP}-280	V_{LR}-320	V_{SO}-850	G_3-110	V_{COL}-840
			HYBRID #1			

V_{EE}-815	V_{1A}-112	V_{REF}A-122	V^{+}A-NC	V^{++}A-540	G_1-360	V_{ID}-675
V_{TT}-65	V_{1B}-116	V_{REF}B-190	V^{+}B-300	V^{++}B-570	G_2-510	V_{M}-0
V_{R}-660	V_{R}-400	V_{OP}-245	V_{LR}-320	V_{SO}-760	G_3-190	V_{COL}-300
			HYBRID #2			

TABLE 3.1 POTENTIOMETER SETTINGS FOR HYBRIDS

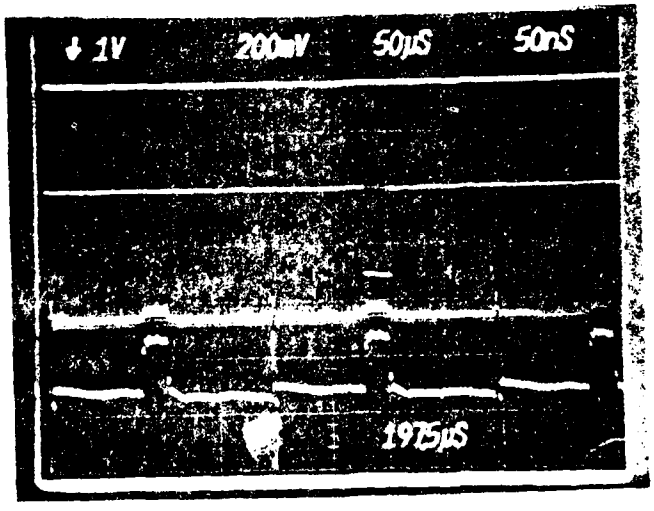


INPUT

EXPANDED INPUT

OUTPUT

HYBRID #1



INPUT

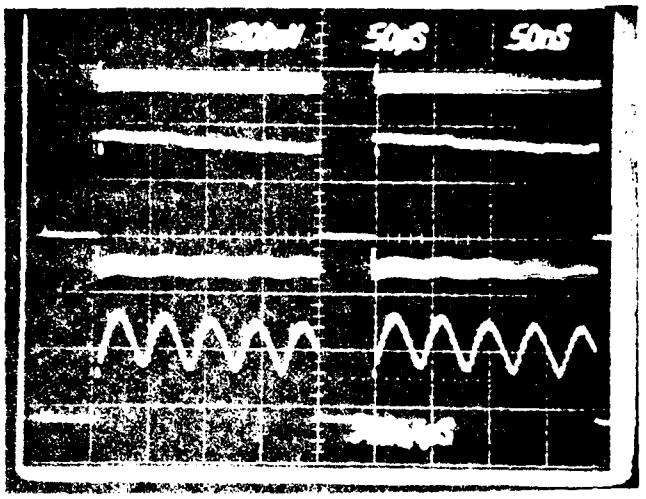
EXPANDED INPUT

OUTPUT

HYBRID #2

FIGURE 3.5

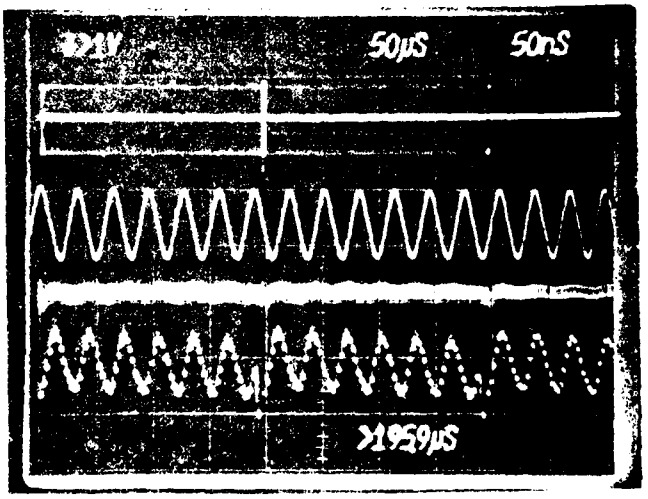
DELIVERED MODULE OPERATION



(A)

FIXED PATTERN
ON OUTPUT

OUTPUT WITH 25 MHZ
TRIANGLE INPUT.



INPUT (GATED 30 MHZ
TRIANGLE)

EXPANDED INPUT

OUTPUT

FIGURE 3.6
TYPICAL OPERATING WAVEFORMS


DATE
ILME